Electronic Version
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Claims

[c1] 1. A split gate flash memory cell, comprising:

a substrate, wherein a device isolation structure is configured in the substrate to define an active region;

a selective gate structure, disposed on the substrate, wherein the selective gate structure comprises, sequentially from the substrate, a gate dielectric layer, a selective gate and a cap layer;

a spacer, disposed on a sidewall of the selective gate structure;

an interlayer dielectric layer, disposed on the substrate, wherein the interlayer dielectric layer comprises an opening, disposed on one side of the selective gate structure, exposing a portion of the selective gate structure, the substrate and the device isolation structure;

a floating gate, disposed in the opening, wherein a portion of the floating gate extends to cover a surface of the interlayer dielectric layer;

a tunneling dielectric layer, disposed between the substrate and the floating gate;

a control gate, formed over the floating gate and disposed in the opening, filling the opening and extending above the selective gate structure;

a gate dielectric layer, disposed between the floating gate and the control gate;
a source region, disposed in the substrate at a side of the control gate that is not adjacent to the selective gate; and
a drain region, disposed in the substrate on a side of the selective gate that is not adjacent to the control gate.

[c2] 2. The memory cell of claim 1 further comprises an erase gate, disposed on the interlayer dielectric layer above the source region, wherein a portion of the erase gate covers the floating gate.

[c3] 3. The memory cell of claim 1, wherein the gate dielectric layer is further disposed between the erase gate and the floating gate.

[c4] 4. The memory cell of claim 1, whereinthe control gate extends to cover the floating gate above the selective gate structure.

[c5] 5. The memory cell of claim 1, wherein an etching selectivity of the cap layer and the spacer is different from that of the interlayer dielectric layer.

[c6] 6. A split gate flash memory device, comprising:
a substrate, wherein a device isolation structure is configured in the substrate to define an active region;

a first selective gate structure and a second selective gate structure, disposed respectively on the substrate, wherein each of the first selective gate structure and the second selective structure comprises a gate dielectric layer, a selective gate and a cap layer;

a spacer, disposed on a sidewall of the first selective gate structure and the second selective gate structure;

an interlayer dielectric layer, disposed on the substrate, wherein the interlayer dielectric layer comprises a first opening and a second opening, and the first opening and the second opening are configured between the first selective gate structure and the second selective gate structure, and the first opening exposes a portion of the first selective gate structure, the substrate and the device isolation structure, and the second opening exposes a portion of the second selective gate structure, the substrate and the device isolation structure;

a first floating gate and a second floating gate, disposed in the first opening and the second opening, respectively, and extended to cover a surface of the interlayer dielectric layer;

a tunneling dielectric layer, disposed between the first floating gate and the substrate, and between the second floating gate and the substrate;

a first control gate and a second control gate, wherein the first and the second control gates are disposed in the

first opening and the second opening, respectively, the first and the second control gates fill the first opening and the second opening, respectively, and the first and the second control gates extend above the first selective gate structure and the second selective gate structure, respectively;

an erase gate, disposed on the interlayer dielectric layer that is in between the first control gate and the second control gate, wherein a portion of the erase gate covers the first floating gate and the second floating gate;

a gate dielectric layer, disposed between the first floating gate and the first control gate and between the first floating gate and the erase gate, and between the second floating gate and the second control gate and between the second floating gate and the erase gate;

a source region, disposed in the substrate between the first control gate and the second control gate;

a first drain region and a second drain region, configured in the substrate, at one side of the first selective gate that is not adjacent to the first control gate, and at one side of the second selective gate that is not adjacent to the second control gate; and

a bit line, disposed on a substrate and electrically connected to the first drain region and the second drain region.

[c7] 7. The memory cell of claim 6, wherein the gate dielectric layer comprises a silicon oxide/silicon nitride/silicon oxide layer.

[c8] 8. The method of claim 6, wherein the first control gate covers the first floating gate above the first selective gate structure, and the second control gate covers the second floating gate above the second selective gate structure.

[c9] 9. The method of claim 6, wherein the bit line is electrically connected to the first drain region and the second drain region through a contact plug, respectively.

[c10] 10. The method of claim 6, wherein an etching selectivity of the cap layer and the spacer is different from that of the interlayer dielectric layer.

[c11] 11. A fabrication method for a split gate flash memory cell, comprising:
providing a substrate, wherein the substrate is already formed with a device isolation structure;
forming a selective gate structure on the substrate, the selective gate structure comprises a gate dielectric layer, a conductive layer and a cap layer;
forming a spacer on a sidewall of the selective gate structure;

forming a source region and a drain region in the substrate beside both sides of the selective gate structure, wherein the source region is at a certain distance away from the selective gate structure, and the drain region is adjacent to the selective gate structure;
forming an interlayer dielectric layer on the substrate;
forming an opening in the interlayer dielectric layer, wherein the opening exposes the substrate between the selective gate structure and the source region, a portion of the selective gate structure and the device isolation structure;
forming a tunneling dielectric layer on the substrate that is exposed by the opening;
forming a floating gate in the opening, wherein the floating gate extends to a part of the interlayer dielectric layer;
forming a gate dielectric layer on the substrate; and
forming a control gate on the substrate, wherein the control gate fills the opening.

[c12] 12. The method of claim 11, wherein the step of forming the control gate on the substrate further comprises:
forming a first conductive layer on the substrate, wherein the first conductive layer fills the opening; and
patterning the first conductive layer to form the control gate.

[c13] 13. The method of claim 12, wherein the control gate covers the floating gate above the selective gate structure.

[c14] 14. The method of claim 12, wherein the step of patterning the first conductive layer to form the control gate further comprises concurrently forming an erase gate on the substrate, wherein a portion of the erase gate covers the floating gate.

[c15] 15. The method of claim 11, wherein forming the gate dielectric layer on the substrate further comprises:
forming a composite dielectric layer on the substrate;
patterning the composite dielectric layer, wherein only the composite dielectric layer disposed on a surface of the floating gate remains; and
forming a dielectric layer on the substrate.

[c16] 16. The method of claim 15, wherein forming the composite dielectric layer on the substrate further comprises:
forming a first silicon oxide layer on the substrate using a thermal oxidation method;
forming a silicon nitride layer on the first silicon oxide layer using a chemical vapor deposition method; and
forming a second silicon oxide layer on the silicon nitride layer using a chemical vapor deposition method.

[c17] 17. The method of claim 11, wherein forming the opening in the floating gate further comprises:
forming a second conductive layer on the substrate; and
patterning the second conductive layer to form the floating gate.

[c18] 18. The method of claim 11, wherein forming the opening in the interlayer dielectric layer comprises:
forming a patterned photoresist layer on the substrate;
removing a portion of the interlayer dielectric layer to form the opening using the patterned photoresist layer, the cap layer and the spacer as a mask.

[c19] 19. The method of claim 11, wherein subsequent to the step of forming the selective gate structure on the substrate, and before the step forming the spacer on the sidewall of the selective gate structure, the method further comprises forming a first lightly doped region and a second lightly doped region in the substrate beside both sides of the selective gate structure, wherein the first lightly doped region is at a certain distance away from the selective gate structure, and the second lightly doped region is adjacent to the selective gate structure.

[c20] 20. The method of claim 11, wherein forming the spacer on the sidewall of the selective gate structure further

comprises:

forming an insulating material on the substrate; and

performing an anisotropic etching process to remove a portion of the insulating material.